Amendments to the Specification

At p. 4, please replace the paragraph beginning at line 5 and ending at line 11 with the following amended paragraph(s):

a plurality of array waveguides provided on the substrate, each array waveguide having a waveguide core formed on the first cladding layer so that the waveguide core substantially covers the mesa formation; a second cladding layer formed over the waveguide cores and the first cladding layer; and wherein the height of the mesa formation is in the range of about 2 to about ~~4.m~~ 4μm; the stress in the second cladding layer is in the range of -20 to +10 MPascals; and the width of the waveguide cores in a direction parallel to the plane of the substrate is in the range of 5.80 to ~~6.20.m~~ 6.20μm.

At p. 5, please replace the 3 paragraphs beginning at line 13 and ending at line 31 with the following amended paragraph(s):

Referring now to the drawings, FIGS. 1a to 1f are schematic cross-sectional illustrations of process steps in the fabrication of part of an integrated optical device according to an embodiment of the invention. In prototype investigations, a 40 channel arrayed waveguide grating (AWG) having a 100 GHz channel spacing and ~~250.m~~ 250μm output waveguide pitch was fabricated, but in other embodiments of the invention many types of optical signal handling devices may be fabricated using this technique, such as variable optical attenuators, optical

switches or routers and/or optical filters. The technique is generally applicable to any integrated optical component using a waveguide structure.

FIG. 1a schematically illustrates a silicon substrate 10 on which a ~~16.m~~ 16μm thick thermal oxide undercladding layer 20 is grown. (It is noted that FIGS. 1a to 1f are highly schematic and in any event not to scale).

In FIG. 1c, a layer of waveguide core glass 30 is deposited, for example by flame hydrolysis deposition (FHD). In a preferred embodiment, the layer 30 is ~~6.m~~ 6μm thick after an annealing stage to consolidate the FHD-deposited material. A mask 40 is applied to mask the path of a desired waveguide core. The mask is preferably formed by photolithographically spinning and exposing a resist layer, followed by development and coating with a metal layer by evaporation. The resist and its cover of metal can be lifted off with acetone to leave the metal mask 40.

At p. 5, please replace the paragraph beginning at line 3 and ending at line 6 with the following amended paragraph(s):

The etching step etches away parts of the core material layer 30 not covered by the mask 40, that is to say, regions forming the complement of the desired waveguide path are removed from the core material layer 30. This leaves a substantially square section ~~(6.m x 6.m)~~ (6μm x 6μm) core 50.

At p. 6, please replace the 2 paragraphs beginning at line 11 and ending at line 25 with the following amended paragraph(s):

As shown in FIG. 1e, the etching process is carried on so that part of the undercladding layer 20 is etched away in regions not protected by the mask 40. This "over-etching" process leaves an undercladding layer 20 which is thinner across most of the device, but which forms a mesa formation 60 substantially covered by the core 50. The height of the mesa formation may also be equivalently referred to as an "over-etch depth" and may typically be in the range of ~~2.m to 3.m~~ 2μm to 3μm, but preferably in any event greater than ~~1.m~~ 1μm.

Finally, in FIG. 1f the mask 40 is removed by conventional techniques and the waveguide and undercladding are covered by an overcladding layer 70. In this prototype embodiment the overcladding layer 70 is ~~22.m~~ 22μm thick (at its thickest) and is a glass formed by FHD deposition using $SiCl_4$, BCl_3 and $POCl_3$. The overcladding composition is such that its refractive index is roughly matched to that of the silica undercladding, and its thermal expansion is slightly higher than that of the silicon substrate (as measured by warpage of coated wafers).

At p. 8, please replace the 2 paragraphs beginning at line 5 and ending at line 19 with the following amended paragraph(s):

In the graph of FIG. 2, the legend indicates first the value of the overcladding lce ($\times 10^{-6}$) followed by the value of the core lce ($\times 10^{-6}$). It can be seen that a zero birefringence is obtained for an over-etch depth of about ~~2.m~~ 2μm upwards using the example parameters. The lowest over-etch depth giving a zero birefringence in this model is obtained for a combination of high lce

for the cladding and low Ice for the core. This model ignores any stress influence due to neighbouring waveguides and also does not consider the index contrast which may have an influence on the ideal over-etch depth.

In order to test the theoretical results, a series of prototype devices constructed as described above were tested. The core birefringence was detected by measuring the filter response or passband for two polarisation states, one parallel to the plane of the substrate and one perpendicular, and detecting the wavelength splitting (in nm) between the two. The results are shown in FIG. 3 which indicate the same generally linear dependence between birefringence and over-etch depth as that predicted by the FEM analysis, crossing the zero-birefringence axis at an over-etch depth of about ~~3:m~~ 3μm.

At pp.8-9, please replace the paragraph beginning at p. 8, line 20 and ending at p. 9, line 19 with the following amended paragraph(s):

Some further investigations have also been carried out to study the influence on the splitting in a 40 channel AWG of other parameters such as the width of the array waveguides in the AWG, the stress in the (over) cladding of the array waveguides, the stress in the core layer from which the array waveguide cores are formed, the refractive index of the core and of the cladding of the array waveguides, and the temperature of the AWG. AWGs are now well known in the art and so the skilled man will already have a full understanding of their structure and operation, for example as reviewed in "PHASAR-based WDM-Devices: Principles, Design and applications", by M. K. Smit, IEEE Journal of Selected Topics in Quantum Electronics Vol2.

No2, June 1996. Splitting measurements were made on individual AWG dies, in-line measurements on wafers were made for other parameters, and corresponding simulations to model the effect of variations in these other parameters on the splitting were also carried out. The AWGs which were measured had glass waveguide cores and cladding formed by FHD deposition, using $SiCl_4$, BCL_3 and $GeCL_4$ for the cores, and $SiCL_4$, BCl_3 and $POCl_3$ for the cladding. For illustrative purposes a typical AWG is shown schematically in FIG. 4 and comprises a ~~die 100~~ die 1 having formed thereon two slab waveguides 110,112 between which are coupled the plurality of array waveguides 120 (only some shown--typically there are about 400 to 600 of them). A plurality of input waveguides 130 are coupled between an input edge 101 of the ~~die 100~~ die 1 (diced from a wafer containing several such die) and a first one 110 of the slab waveguides, and a plurality of output waveguides 140 are coupled between an output edge 102 of the die and the second one 112 of the slab waveguides. The AWG has a 100 GHz channel spacing. The spacing between the output waveguides at the output edge of the die is of the ~~order of 100.m~~ order of 100μm, and the spacing of the input waveguides at the input edge is similar. Both the practical measurements and simulations have shown that both the waveguide width (in a direction parallel to the plane of the substrate), the stress in the (over) cladding and the stress in the core layer have a noticeable effect on the splitting, while the core refractive index and clad index have a relatively insignificant effect on the splitting. As part of these further studies further investigations were also carried out on the correlation between the amount of over-etch (i.e. the mesa height) in the array waveguides and the splitting. The results of all these investigations are presented together below.

At p. 11, please replace the paragraph beginning at line 2 and ending at line 9 with the following amended paragraph(s):

The experimental data was obtained from measurements made on individual AWG structures and/or test structures on wafers from several batches of wafers containing AWG structures, over-etch, stress and core width measurements being taken before the wafers were diced into individual AWG die, and splitting measurements being taken after dicing. Over-etch, stress and core width measurements were taken from about 4 to 5 AWGs on each wafer. Splitting measurements were taken from each AWG die obtained from every batch of wafers. The array pitch in each of the AWG devices was approximately ~~12:m~~ 12μm.

At pp. 11-12, please replace the 2 paragraphs beginning at p. 11 line 28 and ending at p. 12 line 29 with the following amended paragraph(s):

FIG. 5 is a plot of the measured average splitting in channels 2 to 39 for each measured AWG die, plotted against the measured total height H.sub.T ~~(in :m)~~ (in μm) of "waveguide core + over-etch depth" averaged over all the AWGs measured in each batch of wafers of AWGs. Measurements from channels 1 and 40 were not taken in any of the die since these can sometimes produce spurious results which can be misrepresentative of the general trend for the other channels. In all the measured AWGs the height of the core was known to be approx. ~~6:m~~ 6μm. From our simulations and experimental results we believe that variation in the core height will have practically no effect on the splitting (see below). As can be clearly seen from FIG. 5, the best linear fit to the measurements crosses from positive to negative splitting as the total height HT

(and therefore as the over-etch depth) increases. Assuming the core height is ~~6:m~~ 6μm this plot shows a zero splitting will be obtained at an over-etch depth of about ~~3.05:m~~ 3.05μm. FIG. 6 is a plot of the corresponding simulated results for the variation of the splitting with the over-etch depth. For each of three chosen over-etch depths, points are plotted for all the different possible values (which the simulation software can handle) of the other parameters a,b,c,e,f,g,h within the above-mentioned limits. The value of the array pitch, h, used in the simulations was used as a fitting parameter to match the experimental results to those obtained with the model. It was found that a value of ~~h=13.55:m~~ h=13.55μm in the simulations achieved a good match between the two sets of results, as can be seen by comparing FIGS. 5 and 6.

Correlation between Waveguide Width and Splitting

FIG. 7 is a plot of the measured average splitting in channels 2 to 39 for each measured AWG die, against the core width (cd) ~~in :m~~ in μm of the array waveguides (i.e. width of the waveguide core in direction parallel to the plane of the substrate of the AWG die), averaged over all the AWGs measured in each batch of wafers of AWGs. From the resulting linear fit it can be seen that the splitting changes from negative to positive splitting, with increasing waveguide width. FIG. 8 is a graph of the simulated results at three different waveguide widths, again using the array pitch h as a fitting parameter to fit the experimental results to the simulated results. For each of three chosen waveguide core widths, points are plotted for all the different possible values (which the simulation software can handle) of the other parameters a,b,c,d,f,g,h within the above-mentioned limits. Again, the simulation closely matches the measured results.

At pp. 14-15, please replace the 3 paragraphs beginning at p. 14 line 9 and ending at p. 15 line 13 with the following amended paragraph(s):

We also made practical measurements of the variation in the splitting with variation of the temperature of the AWG die. The results of these measurements are plotted in FIGS. 13 to 15, for batches of wafers having positive average splitting, negative average splitting, and where the average splitting changes sign ~~around 40@C~~ around 40°C. (As before, the average splitting of each AWG is calculated as the average splitting over channels 2 to 39 of the AWG die). These graphs clearly show that there is a linear relationship between splitting and temperature, for both positive and negative average splitting, the average splitting increasing linearly with temperature.

The measurements and simulated values obtained above for the splitting with variation of the other parameters were all carried out for room temperature, namely ~~approx. 22@C~~ approx. 22°C. Most AWGs are designed to operate at temperatures between 70 and 80 degrees Celsius. The graphs of FIGS. 13 to 15 indicate that the expected increase in splitting with change in temperature from room temperature ~~(22@C.)~~ (22°C.) to operating temperature ~~(75@C.)~~ (75°C.) is about 7.6 picometres.+-.1.2 picometres. It will thus be apparent that in order to compensate for variation in splitting with temperature, the designer should build in an offset in one or more of the other significant parameters such as the over-etch depth, the cladding stress and/or the waveguide width in order to ensure that the desired splitting value at the normal operating temperature of the AWG will be achieved. In the graphs of FIGS. 5 to 12, a solid straight line has been drawn showing an estimated target splitting of -8 picometres. Aiming for this value of splitting at room temperature, should give the desired (zero or minimal) splitting values at the operating

temperature. From the graphs of simulated and experimental results we would propose that the over-etch depth should be within the range of ~~2.8 to 3.2:m~~ 2.8 to 3.2μm to obtain minimum splitting, for a cladding stress in the range of -10 to 0, preferably about -5, and a waveguide width in the range of ~~5.90 to 6.10:m~~ 5.90 to 6.10μm, preferably about ~~6.00:m~~ 6.00μm, where the array pitch (i.e. average spacing between the array waveguides) ~~h=12:m~~ h=12μm.

Conclusions

From the above it will be appreciated that, in addition to choosing an optimum value for the over-etch depth in order to minimize splitting, the waveguide core width and/or the clad stress and/or the core stress can also be chosen in order to further optimize the splitting, for any chosen depth of over-etch. Additionally, it will be appreciated that one must be careful when choosing values for the depth of over-etch and/or the waveguide width and/or the clad stress or core stress in order to reduce (positive) splitting that one does not choose too large an over-etch which would "overshoot the desired zero splitting condition and result in a negative splitting. From the FIG. 5 graph, the optimum value for the over-etch, appears to be about ~~3:m~~ 3μm.